IN THE CLAIMS:

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Claims 1-12 (canceled)

Claim 13 (currently amended): A system to deskew a parallel data link having a plurality of channels for exchanging digital data, the link comprising:

source and destination nodes with an interconnect medium there between;

a Source Synchronous Driver (SSD) at the link source node to format "M" bits of input data received from core logic and to drive "M" data channels onto the link along with a link clock;

a Dynamic Skew Compensation (DSC) architectural block at the link destination node to receive the "M" data bits and link clock and to compensate for skew, recenter the link clock edge relative to the bits of data, and output "M" bits of data, the DSC block comprising:

a DSC bundle consisting of a plurality of DSC Modules interconnected with a Bundle Interface Module, wherein the DSC Modules perform adjustments to compensate for channel-to-channel skew and substantially center the link clock edge with respect to the data bits;

wherein each DSC Module comprises a plurality of DSC Data Channels and a DSC Clock Channel; and

~~The system of claim 12~~ wherein the DSC Clock channel comprises a Clock Channel Front-End block, Built-In Self-Test Logic, and a utility block.

Claim 14 (original): The system of claim 13 wherein the Clock Channel Front-End block comprises a finite state machine, Clock Image Latch, Image Decode Logic, String-to-Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic.

Claim 15 (currently amended): A system to deskew a parallel data link having a plurality of channels for exchanging digital data, the link comprising:

source and destination nodes with an interconnect medium there between;

a Source Synchronous Driver (SSD) at the link source node to format "M" bits of input data received from core logic and to drive "M" data channels onto the link along with a link clock;

a Dynamic Skew Compensation (DSC) architectural block at the link destination node to receive the "M" data bits and link clock and to compensate for skew, recenter the link clock edge relative to the bits of data, and output "M" bits of data, the DSC block comprising:

a DSC bundle consisting of a plurality of DSC Modules interconnected with a Bundle Interface Module,

wherein the DSC Modules perform adjustments to compensate for channel-to-channel skew and substantially center the link clock edge with respect to the data bits;

wherein each DSC Module comprises a plurality of DSC Data Channels and a DSC Clock Channel; and

~~The system of claim 12~~ wherein each DSC Data Channel comprises a Data Channel Front-End block, Data FIFO, and utility block.~~.~~

Claim 16 (original): The system of claim 15 wherein the Data Channel Front-End block comprises a finite state machine, Data Image Latch, Image Decode Logic, String-to-Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic.

Claim 17 (original): The system of claim 15 wherein the Data FIFO comprises a Pattern Search finite state machine, Data FIFO Register File, FIFO Address Encoder, Write Pointer, Read Pointer, Frame Bit Counter, and Skew Synchronizing Marker Start Sequencer.

Claim 18 (original): The system of claim 17 wherein the Data FIFO Register File is a write-per-bit FIFO.

Claim 19 (currently amended): The system of claim 13 ~~12~~ wherein the DSC bundle performs a cold training sequence.

Claim 20 (currently amended): The system of claim 13 ~~12~~ wherein the DSC bundle performs a warm training sequence.

Claim 21 (new): The system of claim 15 wherein the DSC bundle performs a cold training sequence.

Claim 22 (new): The system of claim 15 wherein the DSC bundle performs a warm training sequence.